State Elements

Slides courtesy of Professor Tod Amon, Southern Utah University, with minor modifications by Nathan Sprague
State Elements

- Unclocked vs. Clocked
- Clocks used in synchronous logic
  - when should an element that contains state be updated?

![Diagram showing clock period, cycle time, rising edge, and falling edge.](image)
An unclocked state element

• The set-reset latch
Latches and Flip-flops

- Change of state (value) is based on the clock:
- Latches: whenever the inputs change, and the clock is asserted
- Flip-flop: state changes only on a clock edge (edge-triggered methodology)
D-latch

- **Two inputs:**
  - the data value to be stored (D)
  - the clock signal (C) indicating when to read & store D

- **Two outputs:**
  - the value of the internal state (Q) and its complement

![D-latch circuit diagram]
D flip-flop

- Output changes only on the clock edge